UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,311	08/27/2003	Sathya P. Kaginele	M4065.0931/P931	4875

24998 7590 03/24/2006

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,311	KAGINELE, SATHYA P.	
	Examiner	Art Unit	
	Christine T. Tu	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003 and 11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003 and 11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant is advised that should claims (1-2, 4-7) be found allowable, claims (24-25, 26-29) will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

2. Applicant is advised that should claims 17-19 be found allowable, claims 30-32 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

3. Applicant is advised that should claims 20-22 be found allowable, claims 33-35 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

4. Claims 1-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

At line 4, the term "said match line under test" lacks antecedent basis. Which match line is being considered as "under test" previously?

At line 8, the phrase "loading a comparand register with said known data pattern" is not interrelated to any steps in the claim.

It is not clear whether or not "an expected result" (at line 11) is coming from the content of the "comparand register" (as being recited at line 8).

Claim 8:

At lines 6 and 9, the term "said match lines (plural)" lacks antecedent basis. Where are these (plurality of) match lines coming from?

Claims 8 and 11:

The use of the word "criterion" (along the claims) should be avoided. It is not clear what particular "criterion" is being recited. In other words, more **specific** situation or condition should be recited instead of just a word "criterion".

Claim 10:

At lines 1-2, the phrase "each set of memory cells is a memory storage location with an address" cannot be understood. It is not clear how can each set of cells (hardware) can be a location with an address (a value).

Claim 12:

It is not clear how the apparatus tests a match line of a memory device as it is recited in the preamble of the claim. In other words, only at least one search line (per CAM memory cell) is compared (as being recited at lines 4-5). No actually testing/comparison on (any part of) the match line is being recited.

Claim 13:

At lines 3-4, it is not clear how and when the condition of "if said match line under test is functioning properly" will occur since no actually test is being performed on the match line in claim 12 (as stated in the rejection for claim 12) (see above paragraph).

Claim 15:

At line 2, the term "said match lines (plural)" lacks antecedent basis. Where are these (plurality of) match lines coming from?

Claim 16:

At line 2, the use of the word "each" should be avoided in the phrase "each said match line". This is because only a single one match line is being recited (at line 1 of claim 12).

Claims 17-18, 20:

The use of the word "criterion" (along the claims) should be avoided. It is not clear what particular "criterion" is being recited. In other words, more **specific** situation or condition should be recited instead of just a word "criterion".

Claim 19:

At lines 3-4, the phrase "enabling circuitry enabling ... in response to said word line" is not logic. It is not clear how the enabling circuitry can perform enabling in response to hardware (said word line). In other words, the enabling circuitry should be in response to some signal(s), not hardware.

Claim 20:

At line 10, the phrase "enabling circuitry enabling ... in response to said word line" is not logic. It is not clear how the enabling circuitry can perform enabling in response to hardware (said word line). In other words, the enabling circuitry should be in response to some signal(s), not hardware.

Claim 23:

It is not clear how the CAM device tests a match line of said CAM device (as it is recited at lines 4-5 of the claim). In other words, only at least one search line (per CAM memory cell) is compared (as being recited at lines 8-9). No actually testing/comparison on (any part of) the match line is being recited.

Claim 24:

At line 8, the phrase "loading a comparand register with said known data pattern" is not interrelated to any steps in the claim.

It is not clear whether or not "an expected result" (at line 11) is coming from the content of the "comparand register" (as being recited at line 8).

Claims 30-31, 33, 36-37, 39:

The use of the word "criterion" (along the claims) should be avoided. It is not clear what particular "criterion" is being recited. In other words, more **specific** situation or condition should be recited instead of just a word "criterion".

Claims 37-38 (each depends on claim **36**):

It is not clear whether each of these claims should depend on claim 36 or claim 39.

Claim 42:

At line 15, the term "said match line under test" lacks antecedent basis. Which match line is being considered as "under test" previously?

It is not clear how the apparatus tests a match line of said CAM device (as it is recited at lines 4-5 of the claim). In other words, only at least one search line (per CAM memory cell) is compared (as being recited at lines 8-9). No actually testing/comparison on (any part of) the match line is being recited.

At line 19, the phrase "loading a comparand register with said known data pattern" is not interrelated to any steps in the claim.

It is not clear whether or not "an expected result" (at line 22) is coming from the content of the "comparand register" (as being recited at line 19).

Claims 2-7, 9-10, 14, 21-22, 25-29, 32, 34-35, 41:

These claims are rejected because they depend on claims 1, 8, 12, 17, 20, 23, 24, 30, 33 and 36 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu (7,002,823).

Claims 1-2:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figures 1 & 5) that, in a CAM device (100), a CAM array (101) includes a plurality of CAM cell arranged in rows for storing CAM words. A comparand register (115) is used to store a comparand value received via the comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, and then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figure 1, column 3 line 29 - column 4 line 34).

Ichiriu states that a decoder (105) inside the CAM device (100) decodes an selected address to activate one of a plurality of word lines (181) (column 5 lines 17-23).

Ichiriu further states that at the start of a comparison operation, feature of precharging each of the match lines (182) to a high logical level (column 6 lines 61-column 7 line 4).

Ichiriu does not explicitly teach the enabling out from the match line under test. Ichiriu, however, teach that unless a host is programmed to read all the locations in the

CAM array, it is likely that numerous CAM array locations will not be checked (column 4 lines 26-29).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM array (101) would have been compared partially instead of comparing all the CAM words in the CAM array (101). One having ordinary skill in the art would be motivated to realize so because Ichiriu states that numerous CAM array locations will likely not to be checked (column 4 lines 26-29).

Claim 3:

Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Claims 4-5:

Ichiriu's decoder (105) is a state machine that transitions from state to state in response to transitions of a clock signal (CLK) (104) (column 4 lines 57-67).

Claims 6-7:

Ichiriu teaches that each row of CAM cells (201) is coupled to a respective match line (182) (figure 5, column 6 lines 33-37).

Claims 8-9 and 11:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 1) that a CAM array (101) includes a plurality of CAM cell arranged in rows for storing CAM words. A comparand register (115) is used to store a comparand value received via the comparand bus (143) and outputs the comparand value to the CAM array (101). During a compare operation, the comparand may be masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array. Each of the rows of CAM cell is coupled to a corresponding match line (182) and any match between the comparand and a valid CAM word results in a match signal being output to the flag circuit (112). The flag circuit (112) then outputs a match flag signal to indicate that a match has occurred (figure 1, column 3 line 29 - column 4 line 34).

Ichiriu does not explicitly teach the enabling of the match line of a set of memory cell. Ichiriu, however, teach that unless a host is programmed to read all the locations in the CAM array, it is likely that numerous CAM array locations will not be checked (column 4 lines 26-29).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Ichiriu's CAM array (101) would have been compared partially instead of comparing all the CAM words in the CAM array (101). One having ordinary skill in the art would be motivated to realize so because Ichiriu states that numerous CAM array locations will likely not to be checked (column 4 lines 26-29).

Claim 10:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claims 12 and 14:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figures 5 and 1) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns, with each row of CAM cells (201) being coupled to a respective word line and to a respectively match line (182). Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal (figure 5, column 6 line 33-column 7 line 13).

Ichiriu does not explicitly teach a circuit coupled to the match line under test, the corresponding word line and a test mode match line reset signal. It would have been obvious to one skilled in the art at the time the invention was made to realize that such a circuit would have been included in Ichiriu's CAM device so that every Ichiriu's match line is precharged to a high logical level for a comparison operation. One having ordinary skill in the art would be motivated to realize so because Ichiriu teaches that each of the match lines (182) is precharged to high logical level at the beginning of a comparison operation (column 6 line 64-column 7 line 4).

Claim 13:

Ichiriu also teaches a priority encoder (114), in responsive to the results of any match between the comparand and a valid CAM word, for outputting a CAM index (174), such a CAM index an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claims 15-16:

Ichiriu teaches that each row of CAM cells (201) is coupled to a respective match line (182) (figure 5, column 6 lines 33-37).

Claims 17-18:

Ichiriu discloses the invention substantially as claimed. Ichiriu shows (figure 5) that a CAM array (101) includes a plurality of CAM cells (201) arranged in rows and columns, with each row of CAM cells (201) being coupled to a respective word line. Each CAM (201) includes a compare circuit to compare the content of the memory cell with a comparand signal (figure 5, column 6 line 33-column 7 line 13).

Ichiriu does not explicitly teach the enabling circuitry for enabling the match lines. It would have been obvious to one skilled in the art at the time the invention was made to realize that a circuitry being named as "enabling circuitry" would have been included in Ichiriu's CAM device so that every Ichiriu's match line is precharged to a high logical level for a comparison operation. One having ordinary skill in the art would be motivated to realize so because Ichiriu teaches that each of the match lines (182) is precharged to high logical level at the beginning of a comparison operation (column 6 line 64-column 7 line 4).

Claim 19:

Ichiriu teaches each row of CAM cells (201) is coupled to a respective word line (181) and to a respective match line (182) (figure 5, column 6 lines 35-37).

Claims 20-21:

These claims are similar to claim 17 and 19 with additional recited control circuitry for resets the enabling circuitry. Ichiriu teaches that the CAM array (101) includes circuitry to force validity value with each validity storage cell (202) to a reset state to prevent assertion of a match signal by pulling the match line low for the corresponding row of CAM cells (column 7 lines 49-65, column 8 lines 20-24).

Claim 22:

Ichiriu teaches that a comparand value is stored to the CAM array (101). Ichiriu also teaches that the results of any match between the comparand and a valid CAM word are outputted to a priority encoder (114) for outputting a CAM index (174), such a CAM index an address of the CAM word corresponding to the selected match signal (column 4 lines 1-8).

Claim 23:

This claim is similar to claim 12 with additional processing system having a processor. Ichiriu shows a system (960) including a CAM device (961), a CPU (962) and a network processing unit (NPU) (963) (figure 38, column 37 lines 26-45).

Claims 24-35:

Claims (24-25, 26-29), (30-32), (33-35) are rejected for reasons similar to those set forth against claims (1-2, 4-7), (17-19), (20-22), respectively.

Claims 36-38:

These claims are similar to claims 17-19 except that a router is being recited. Ichiriu teaches a routing device including a CAM device (961) (figure 38, column 37 lines 26-45).

Claims 39-41:

These claims are similar to claims 20-22 except that a router is being recited. Ichiriu teaches a routing device including a CAM device (961) (figure 38, column 37 lines 26-45).

Claim 42:

This claim is similar to claims 1 and 23 with additional processing system having a processor. Ichiriu shows a system (960) including a CAM device (961), a CPU (962) and a network processing unit (NPU) (963) (figure 38, column 37 lines 26-45).

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2138

March 18, 2006